

Fig. 1

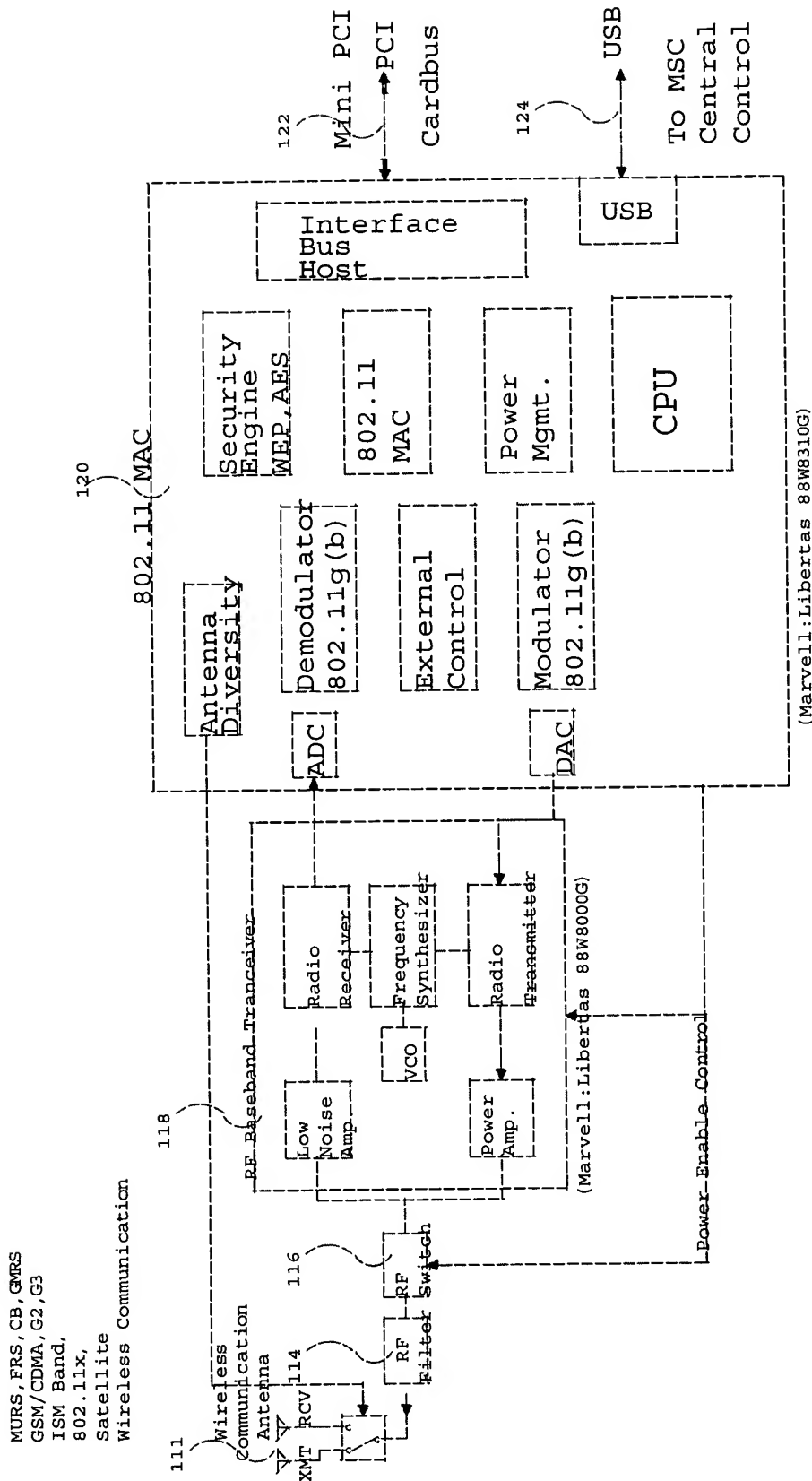


Fig. 2

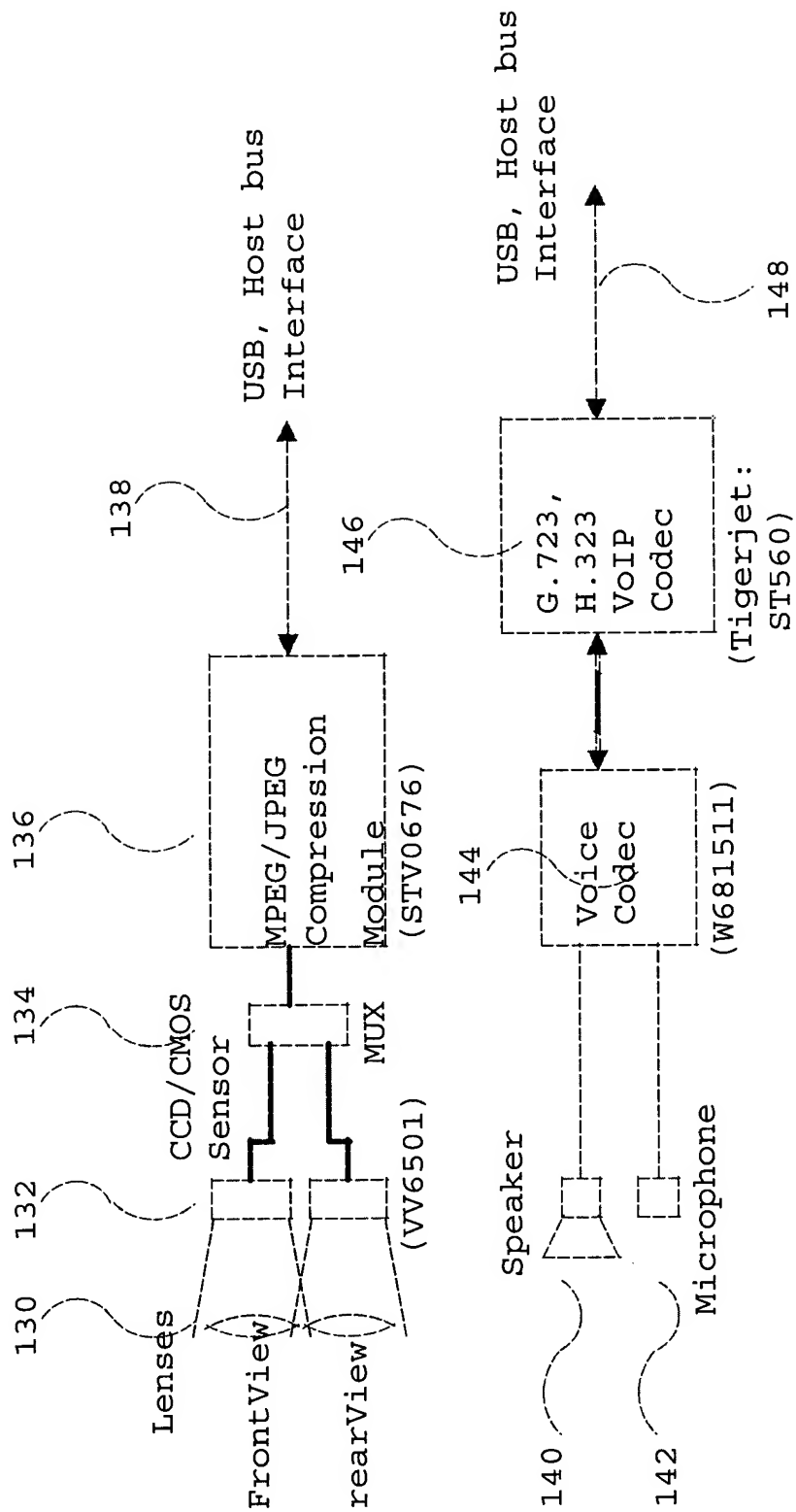


Fig. 3

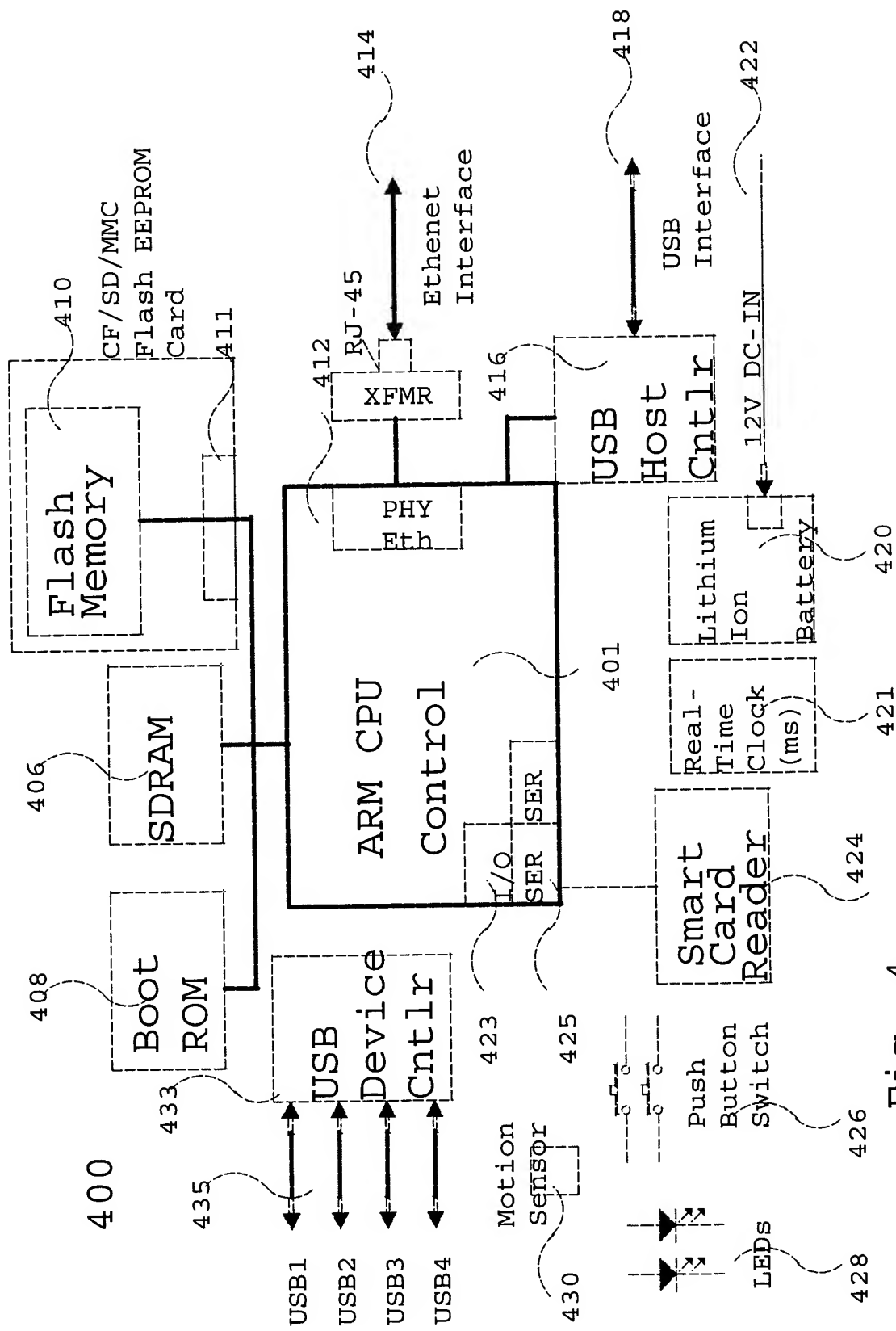


Fig. 4

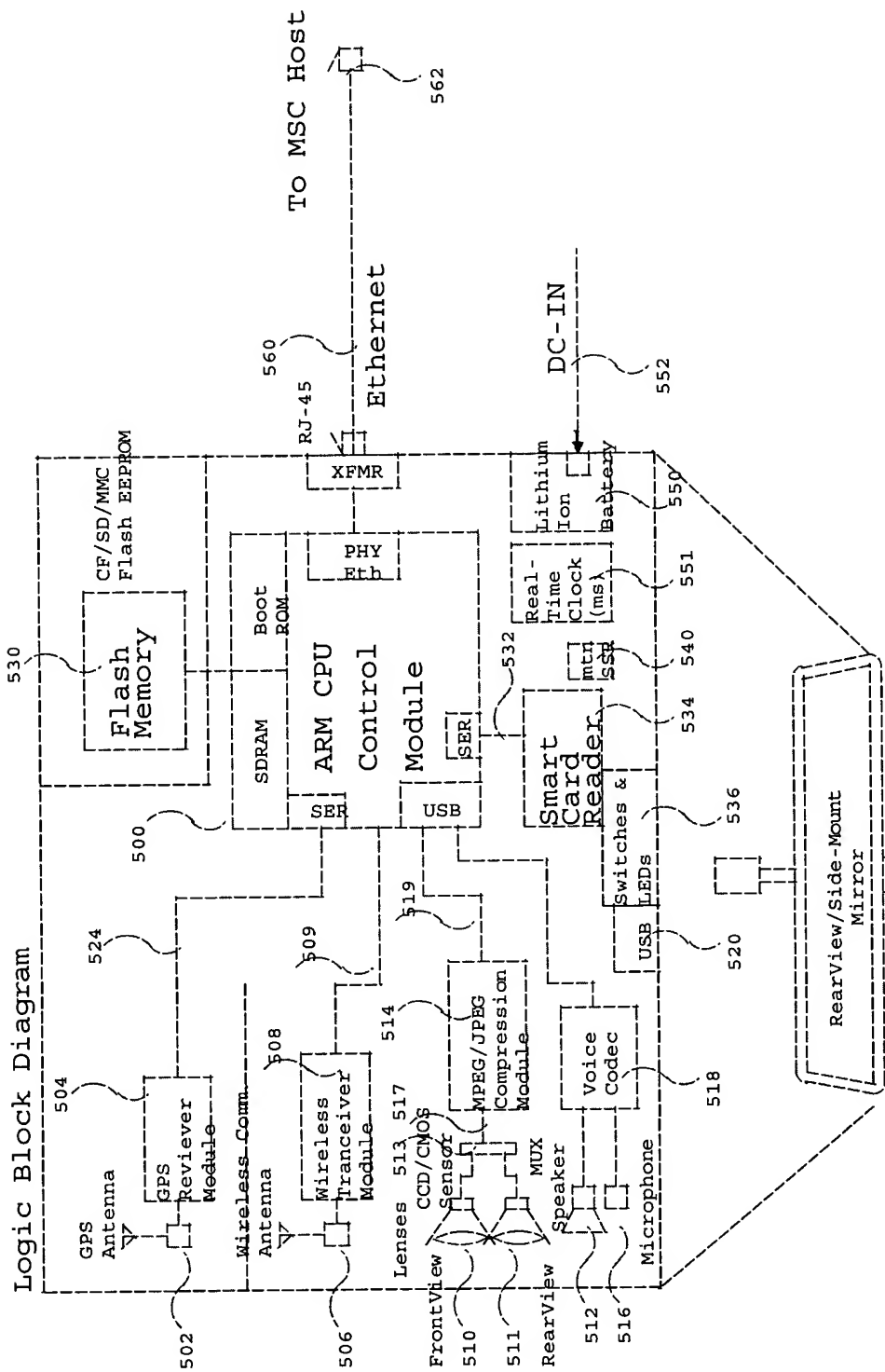


Fig. 5

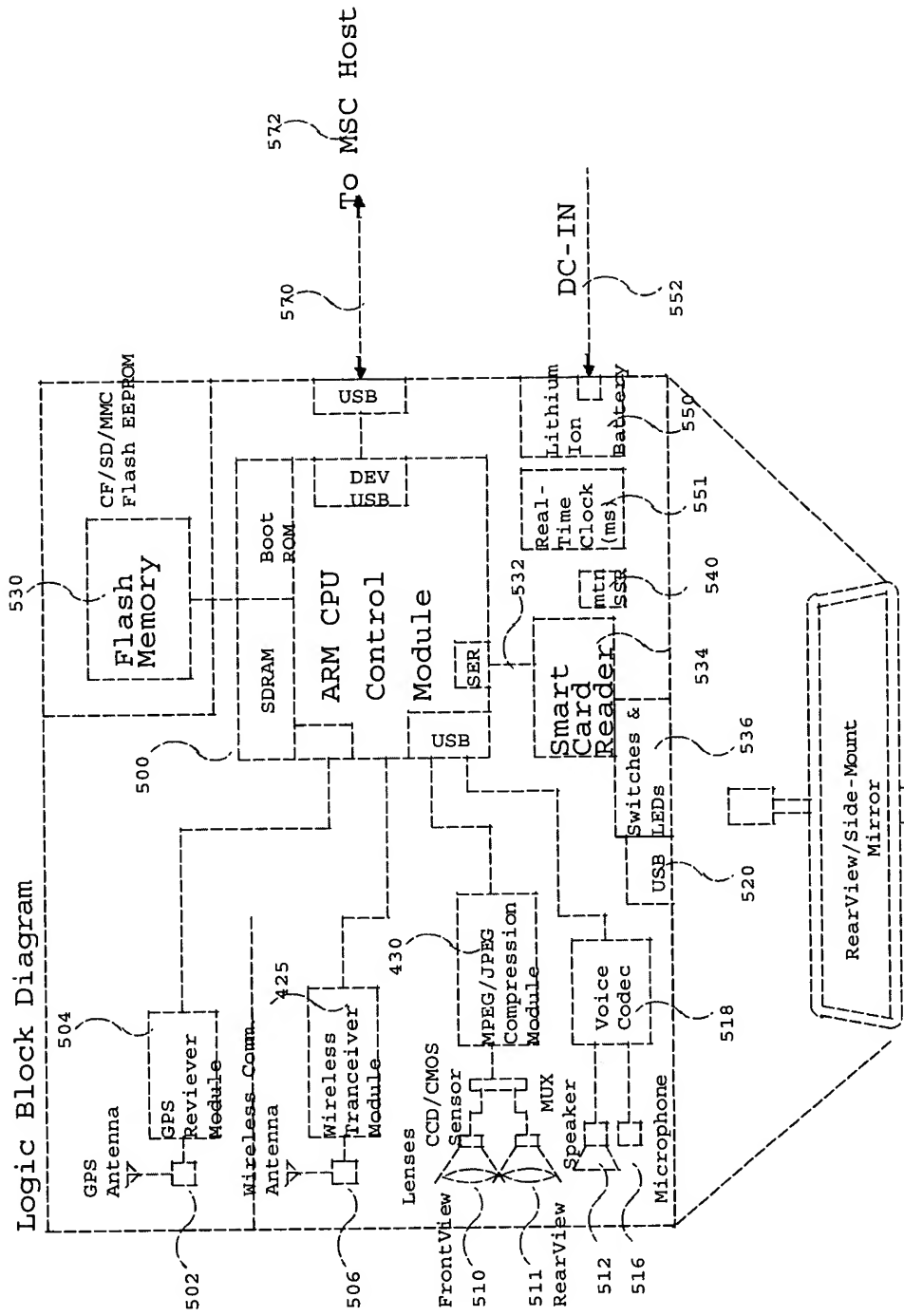
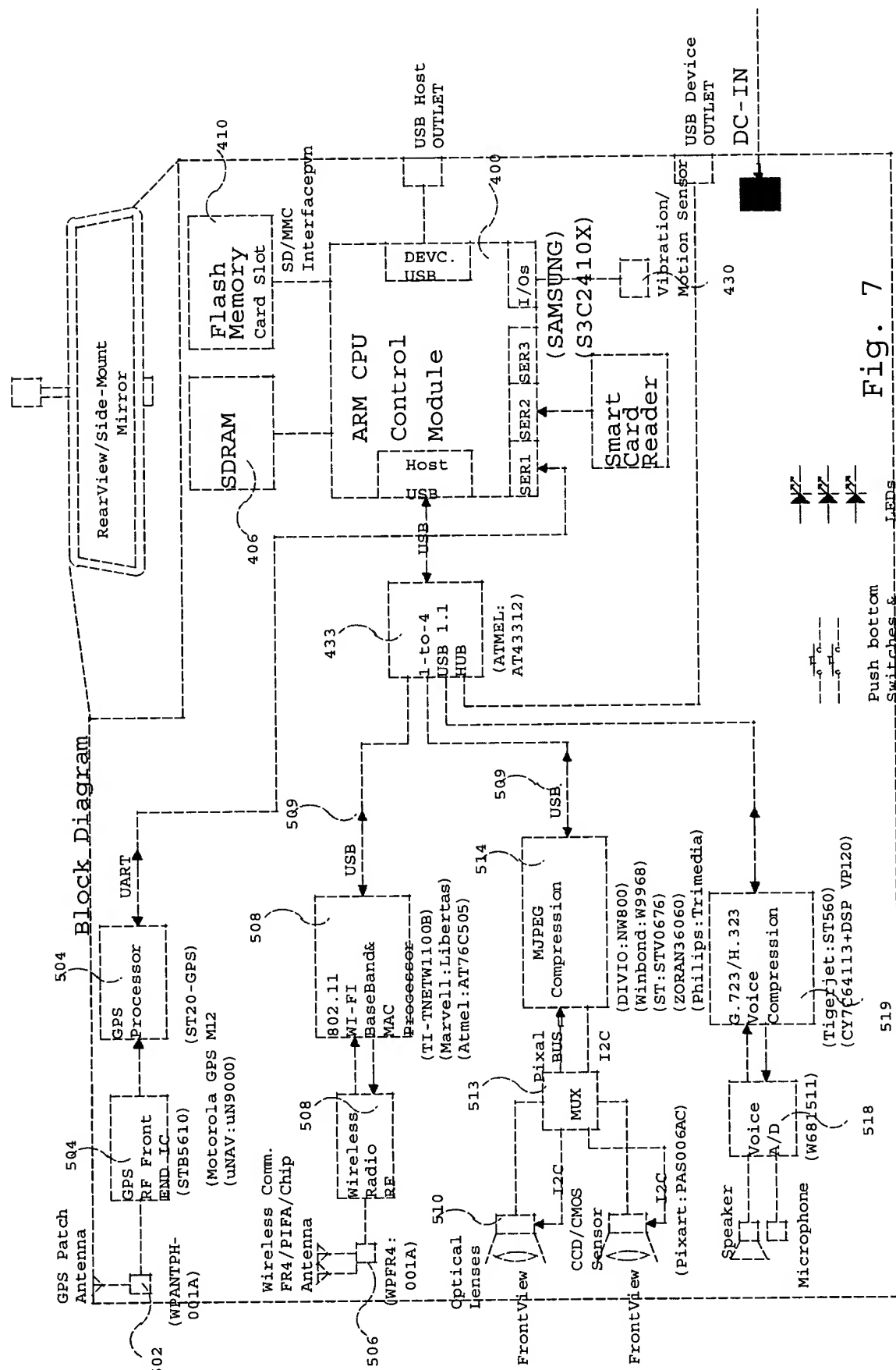


Fig. 6



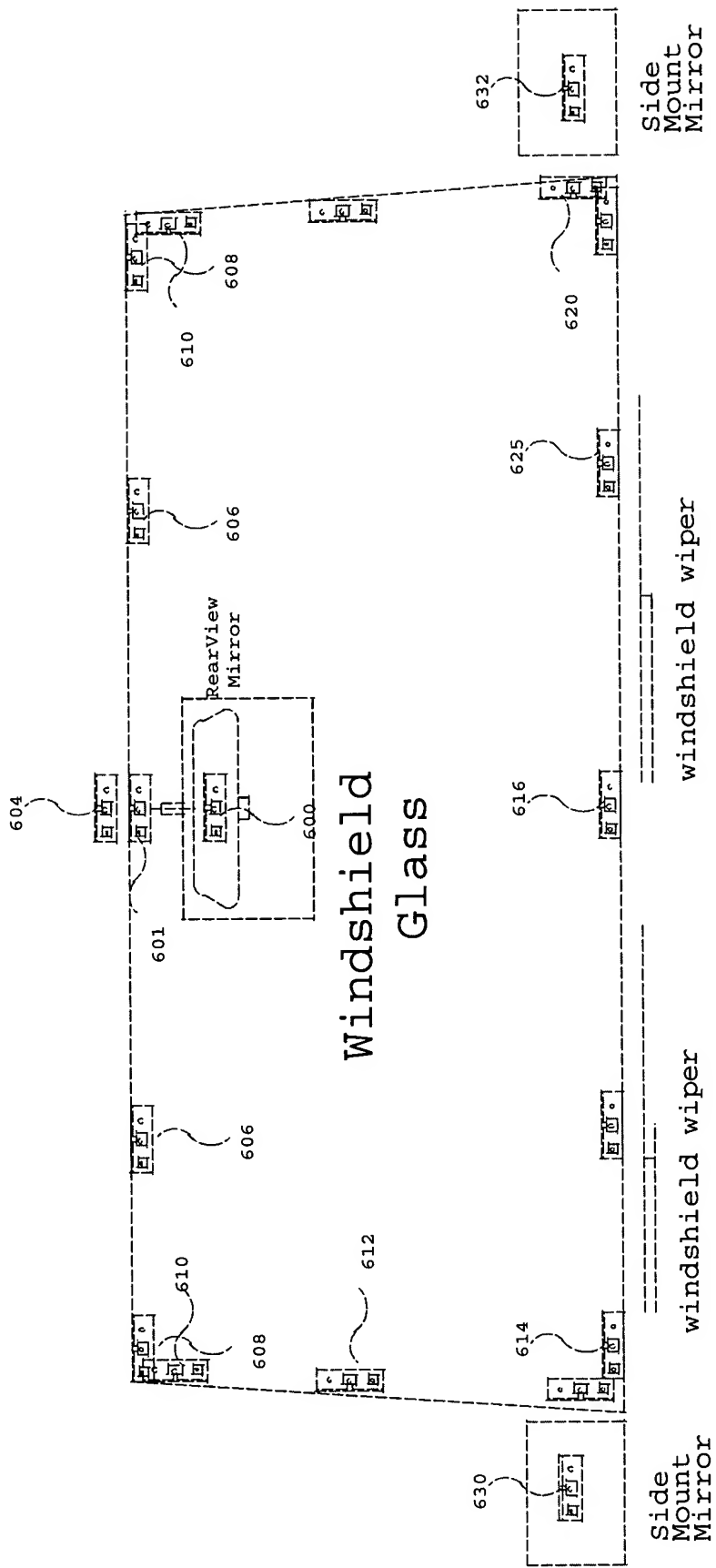


Fig. 8

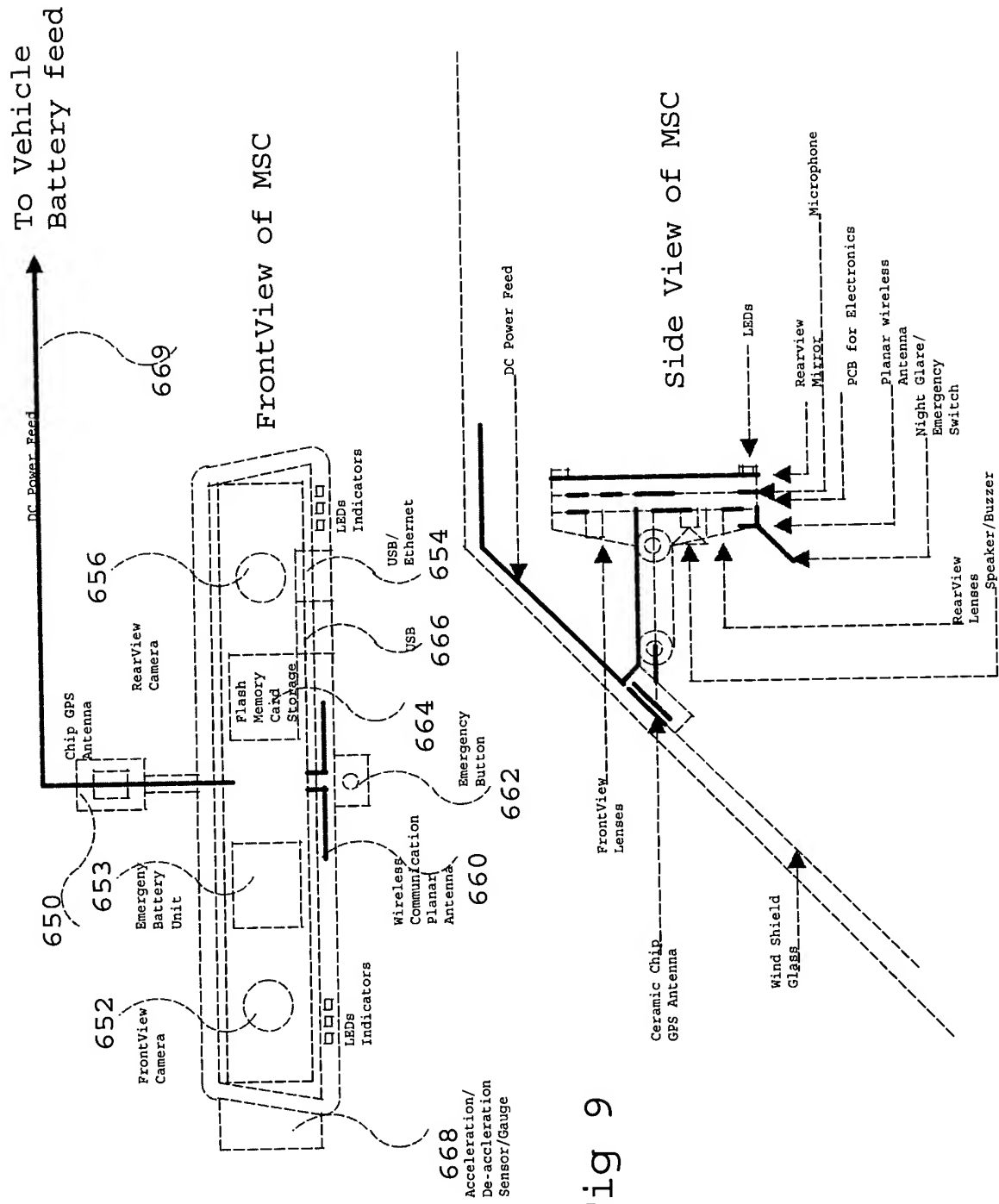


Fig 9

DRAM to Flash Scheme on Significant Events

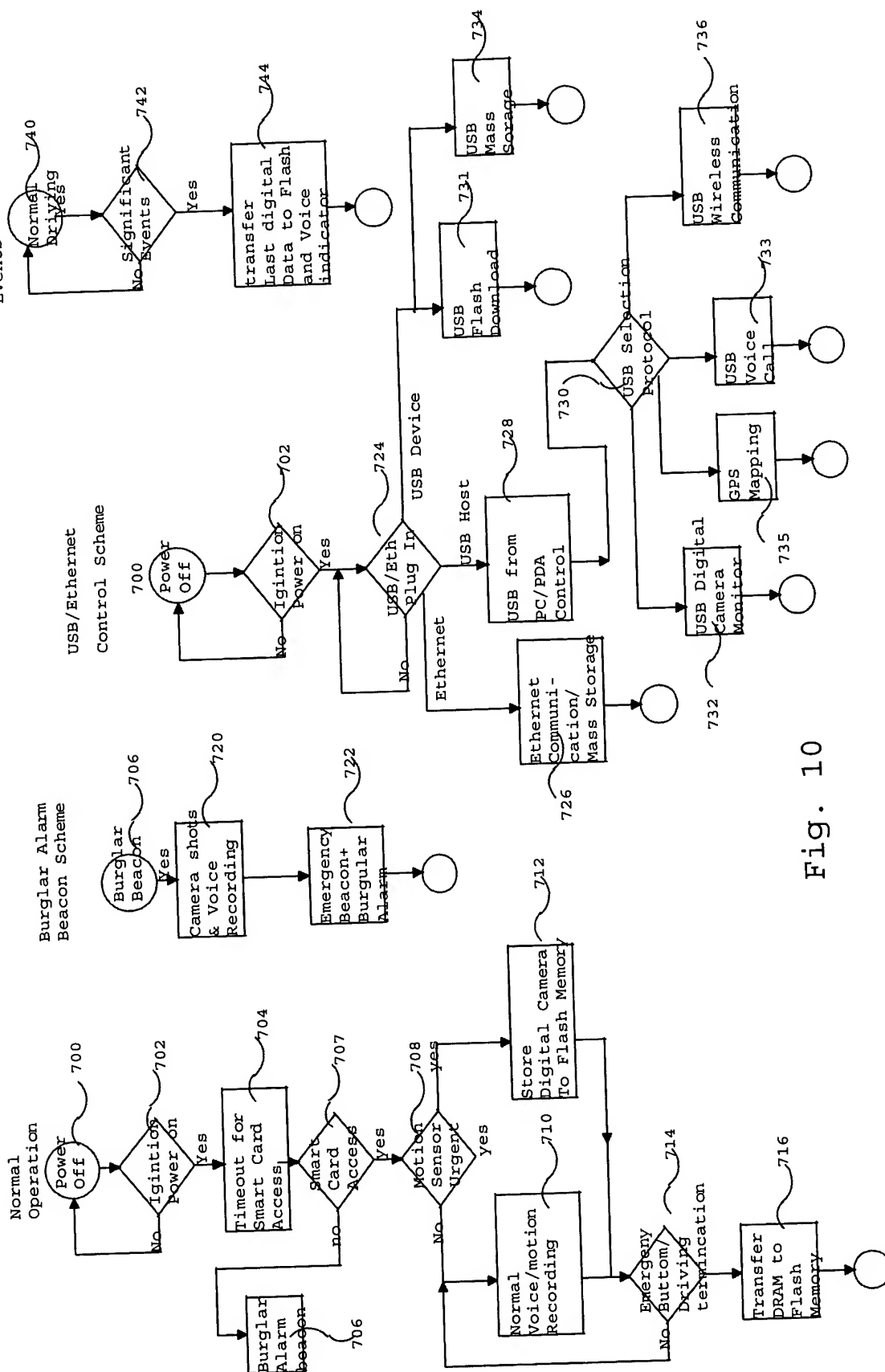


Fig. 10

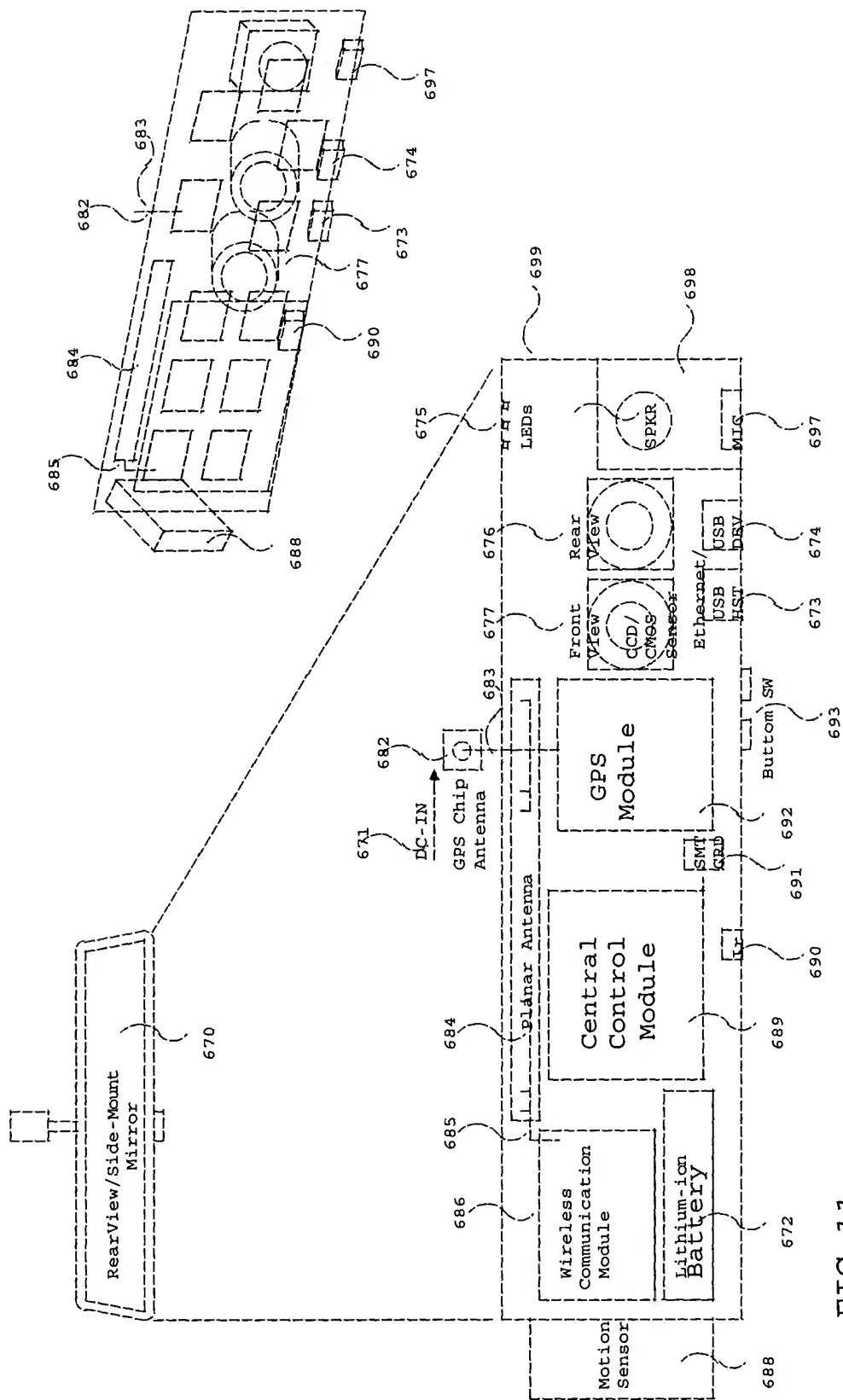


FIG 11:

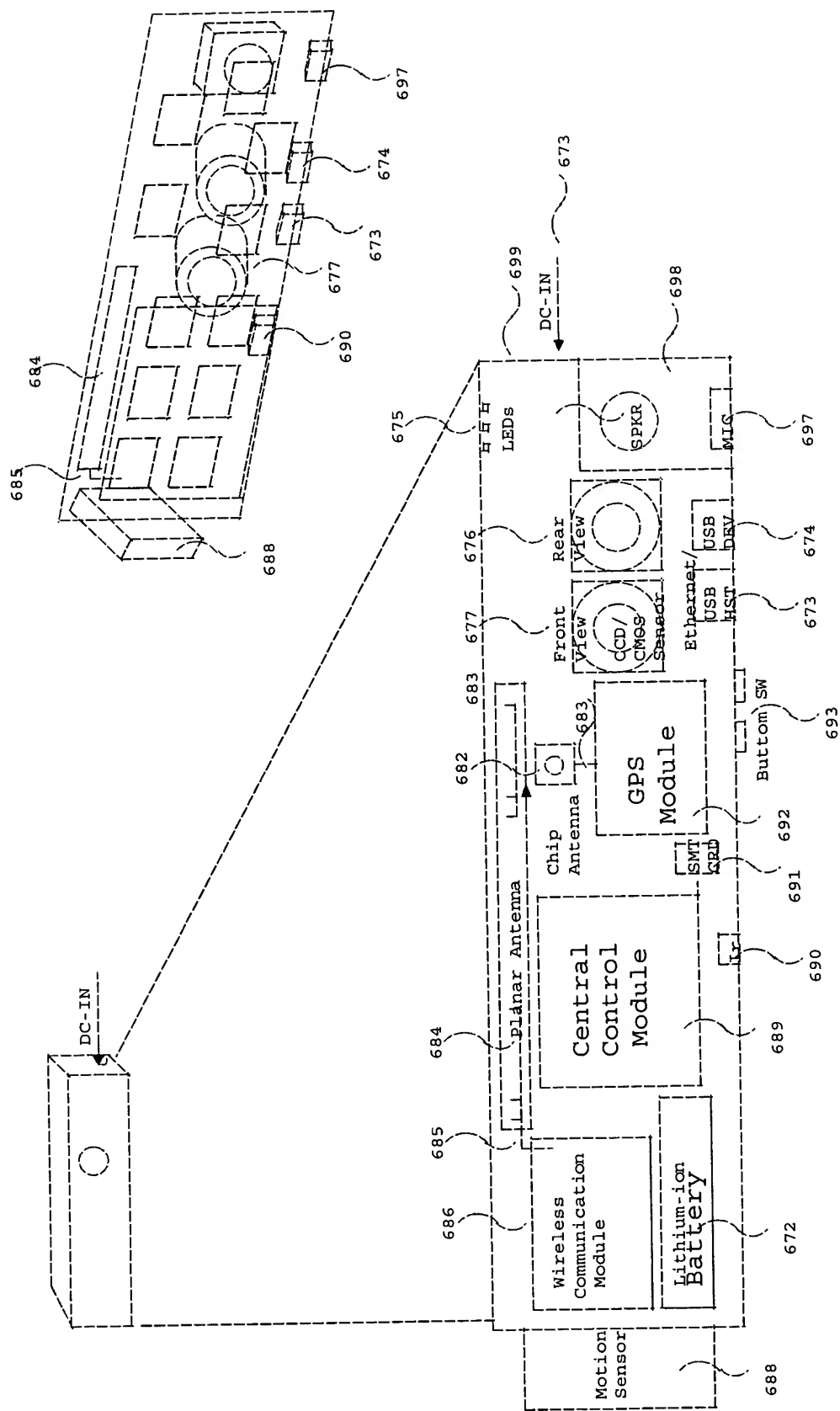


FIG 12:

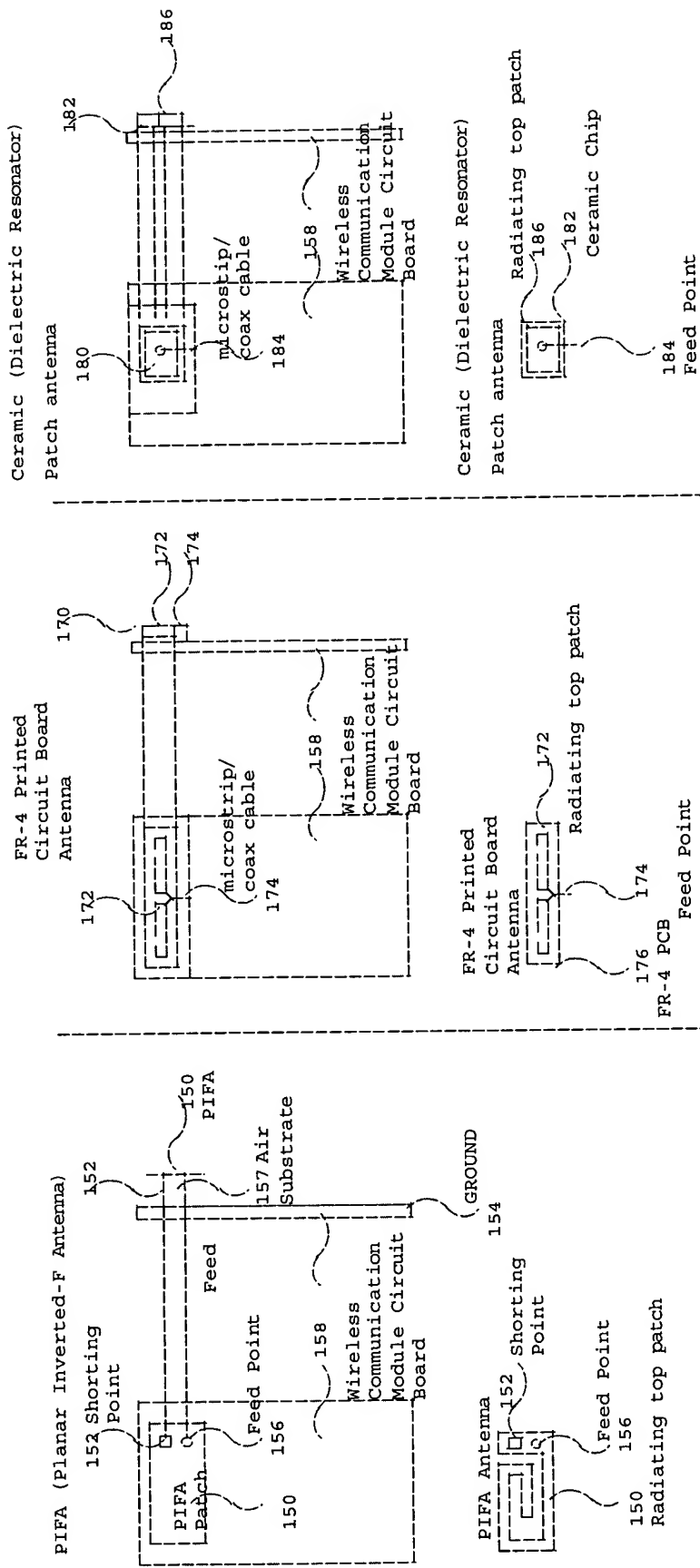


Fig. 13

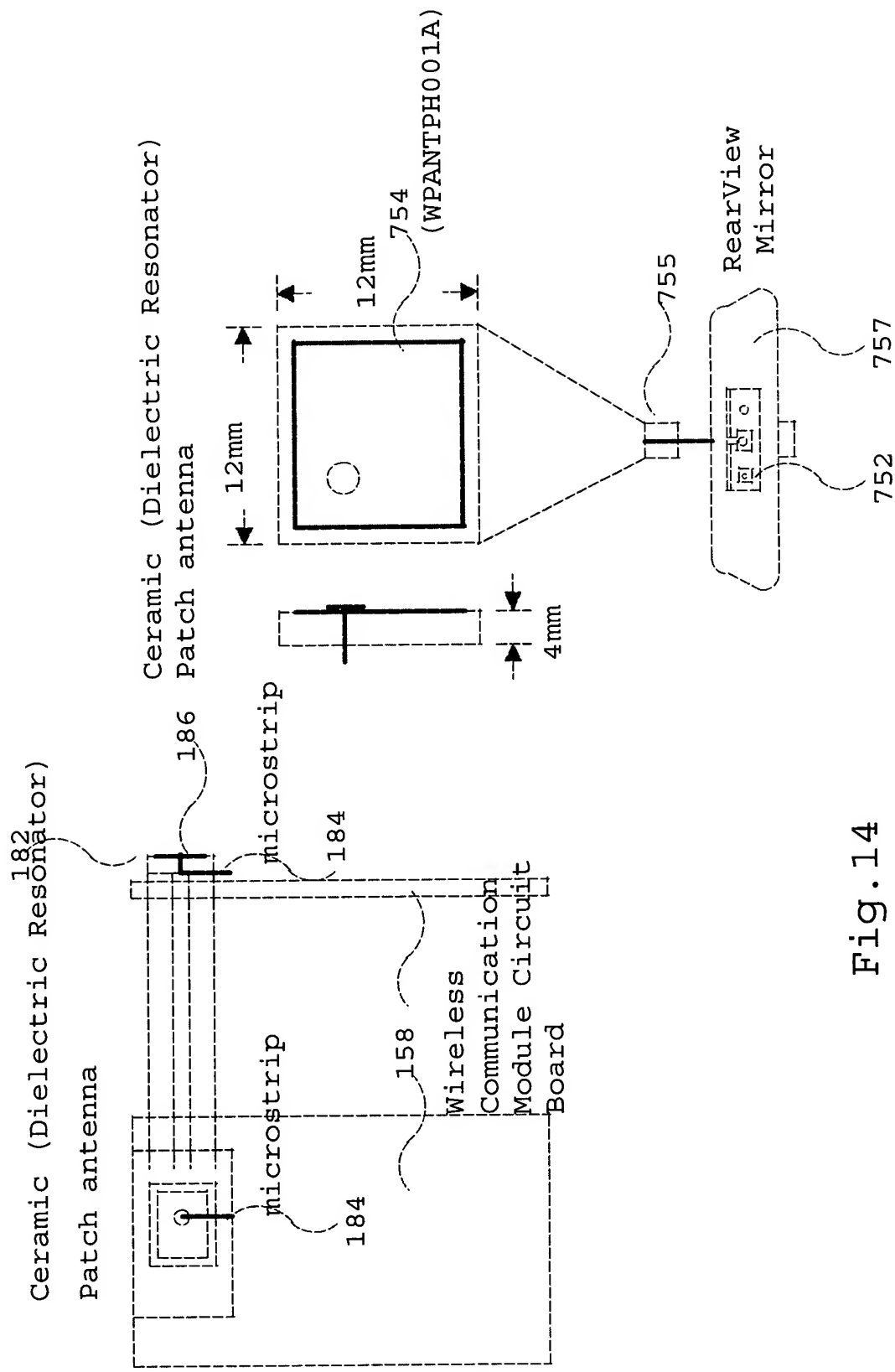


Fig.14

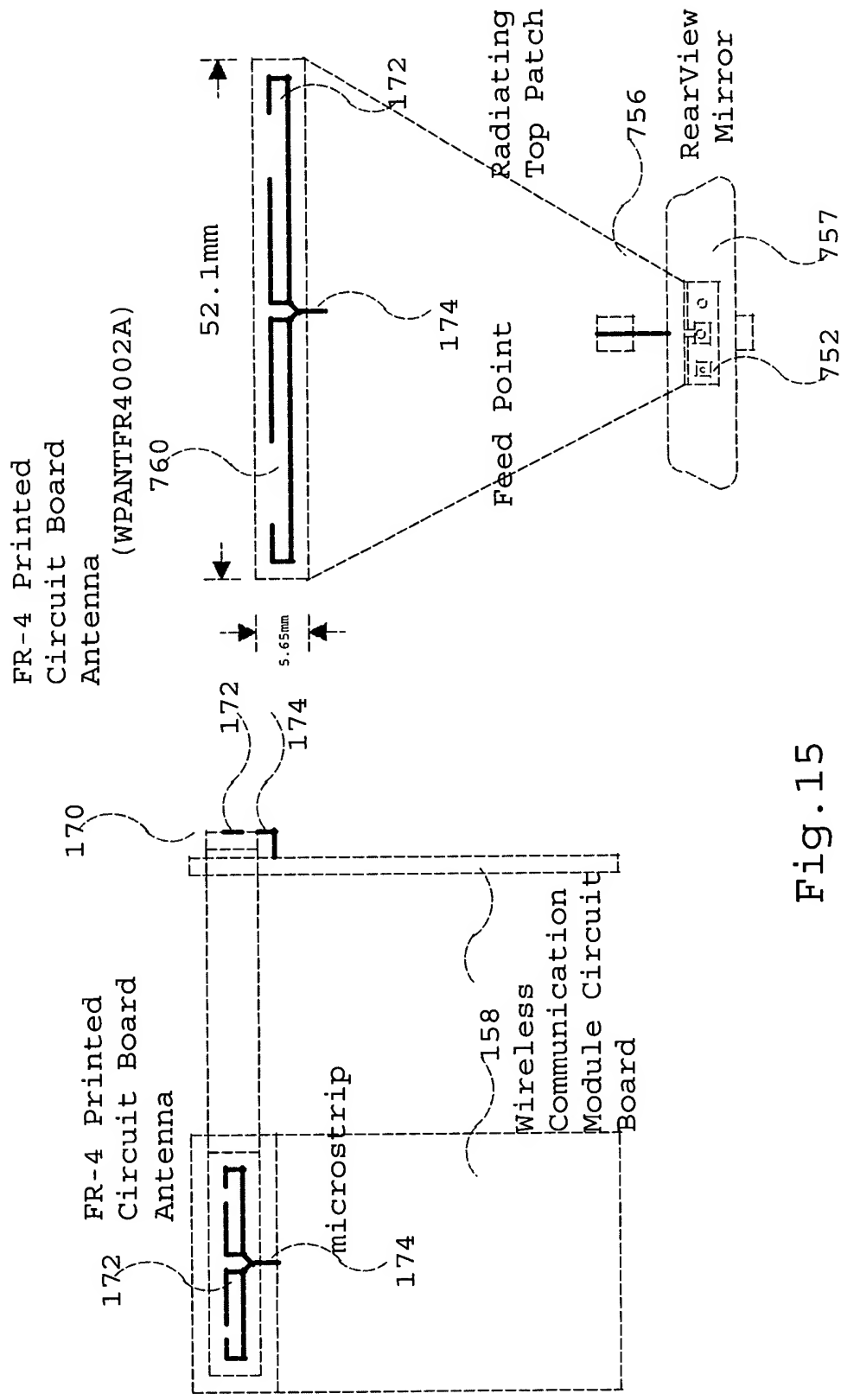


Fig.15

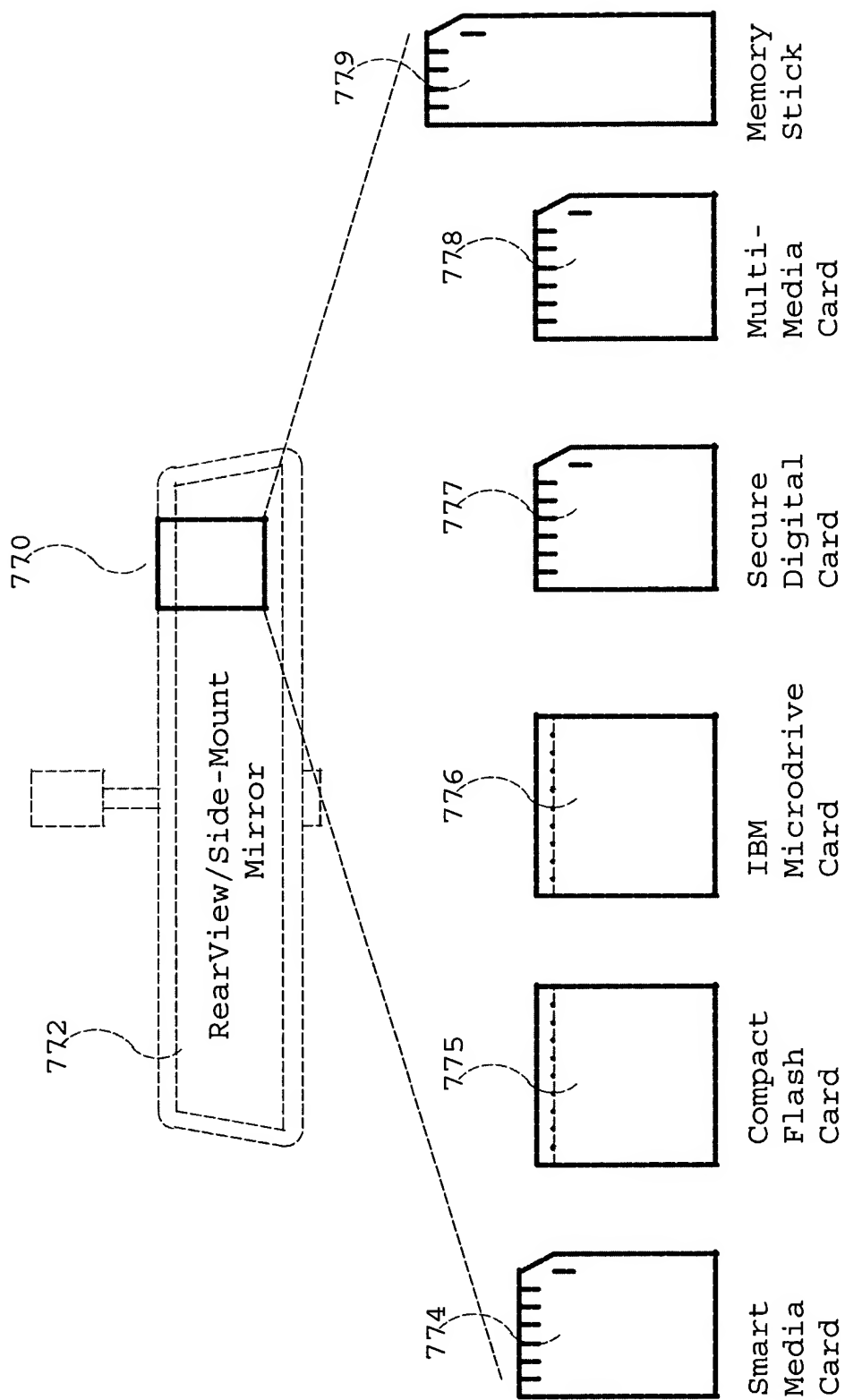


Fig. 16

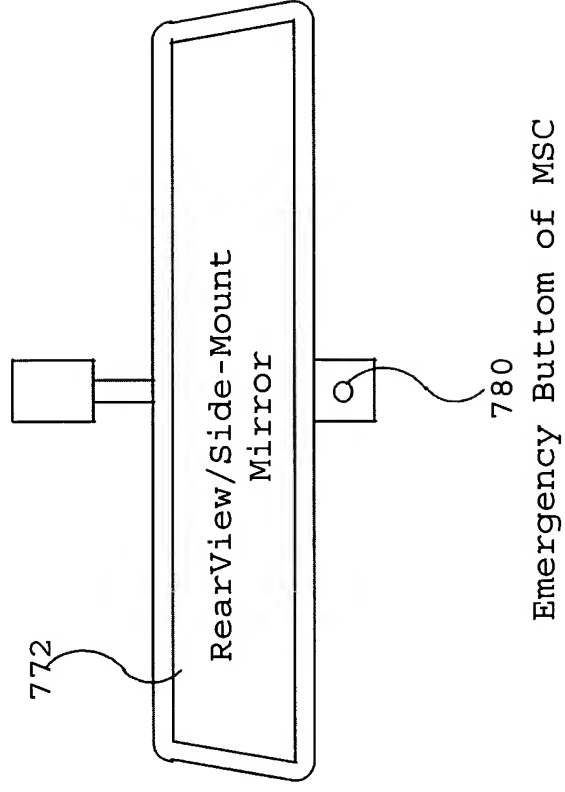


Fig.17

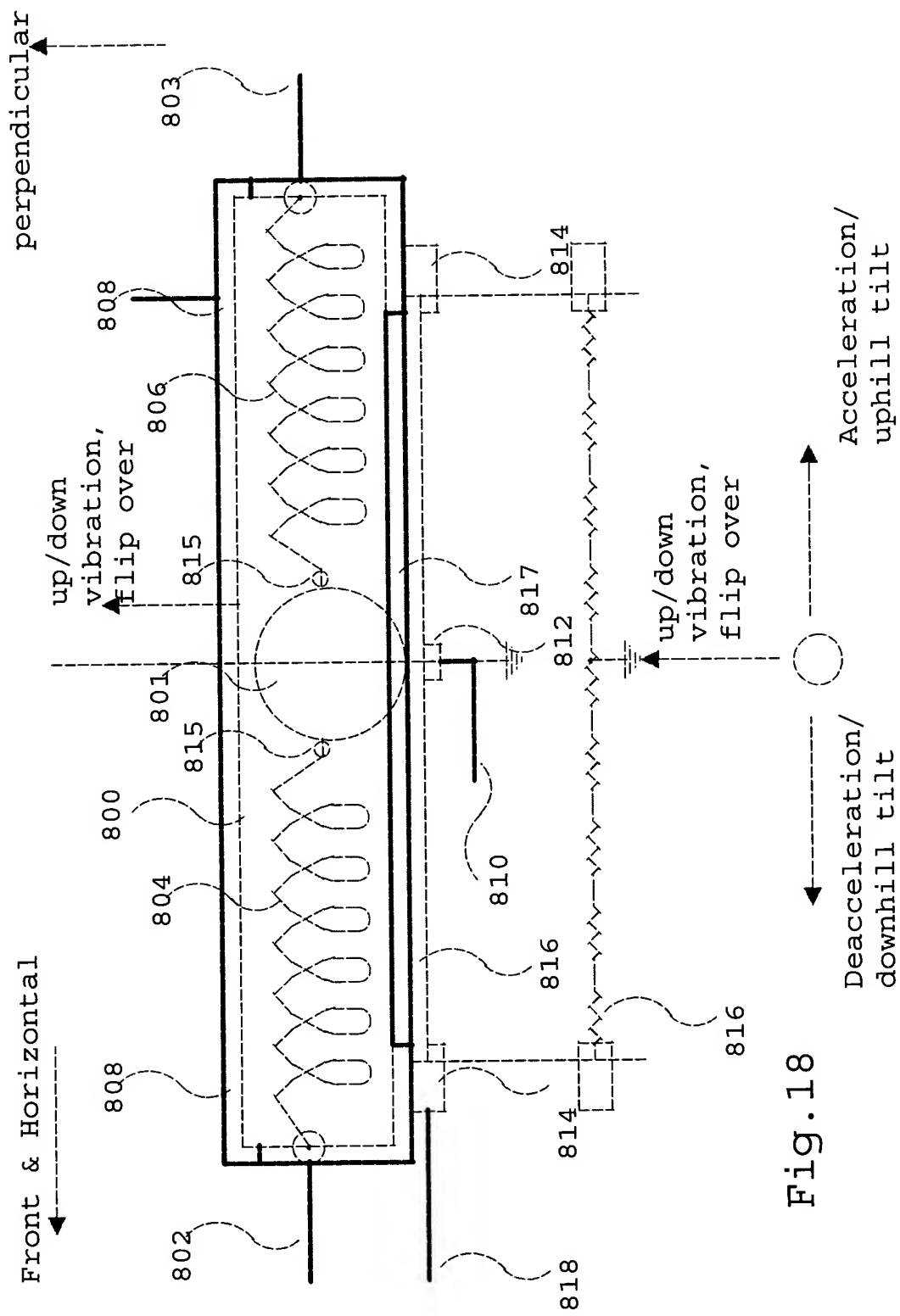


Fig.18

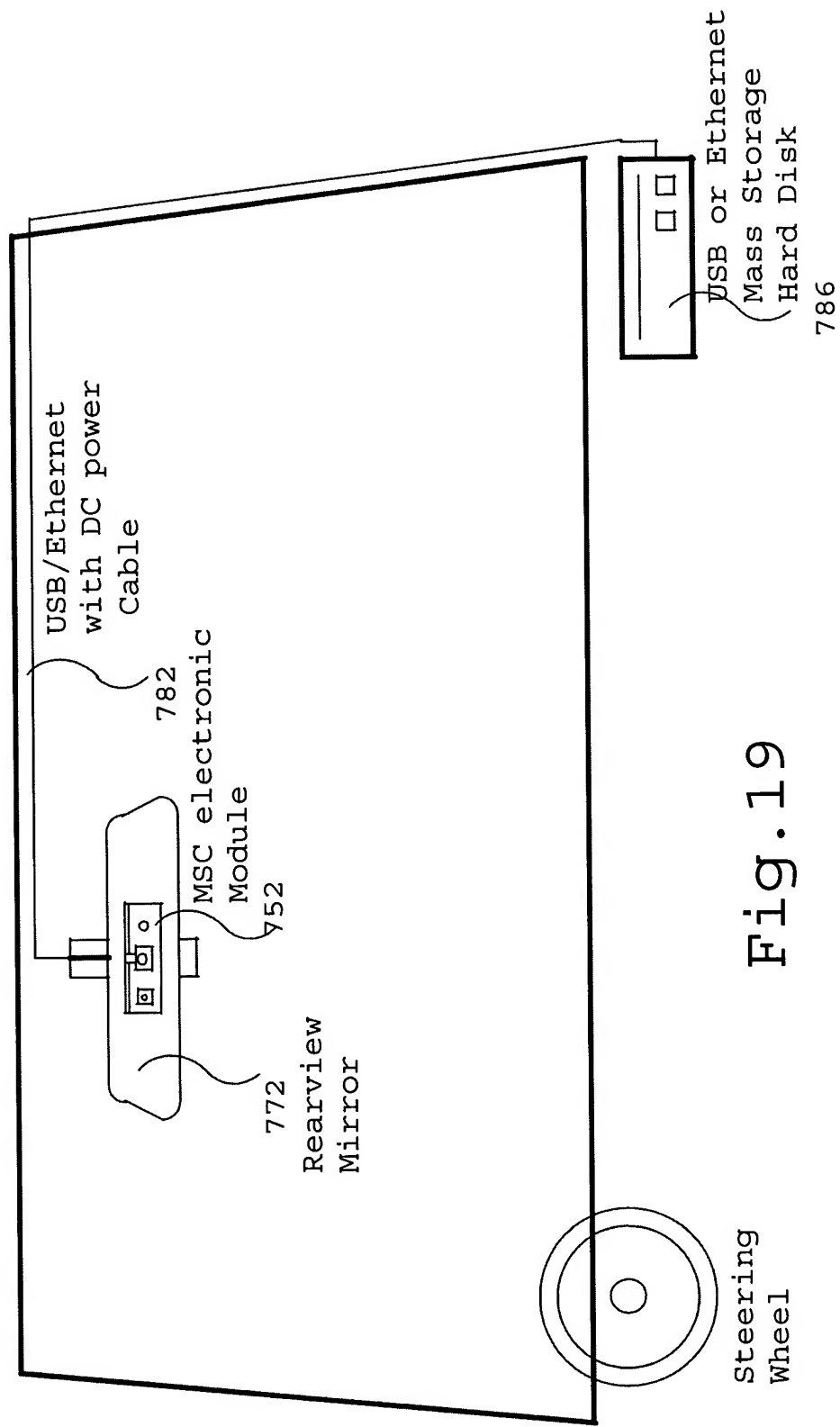


Fig. 19

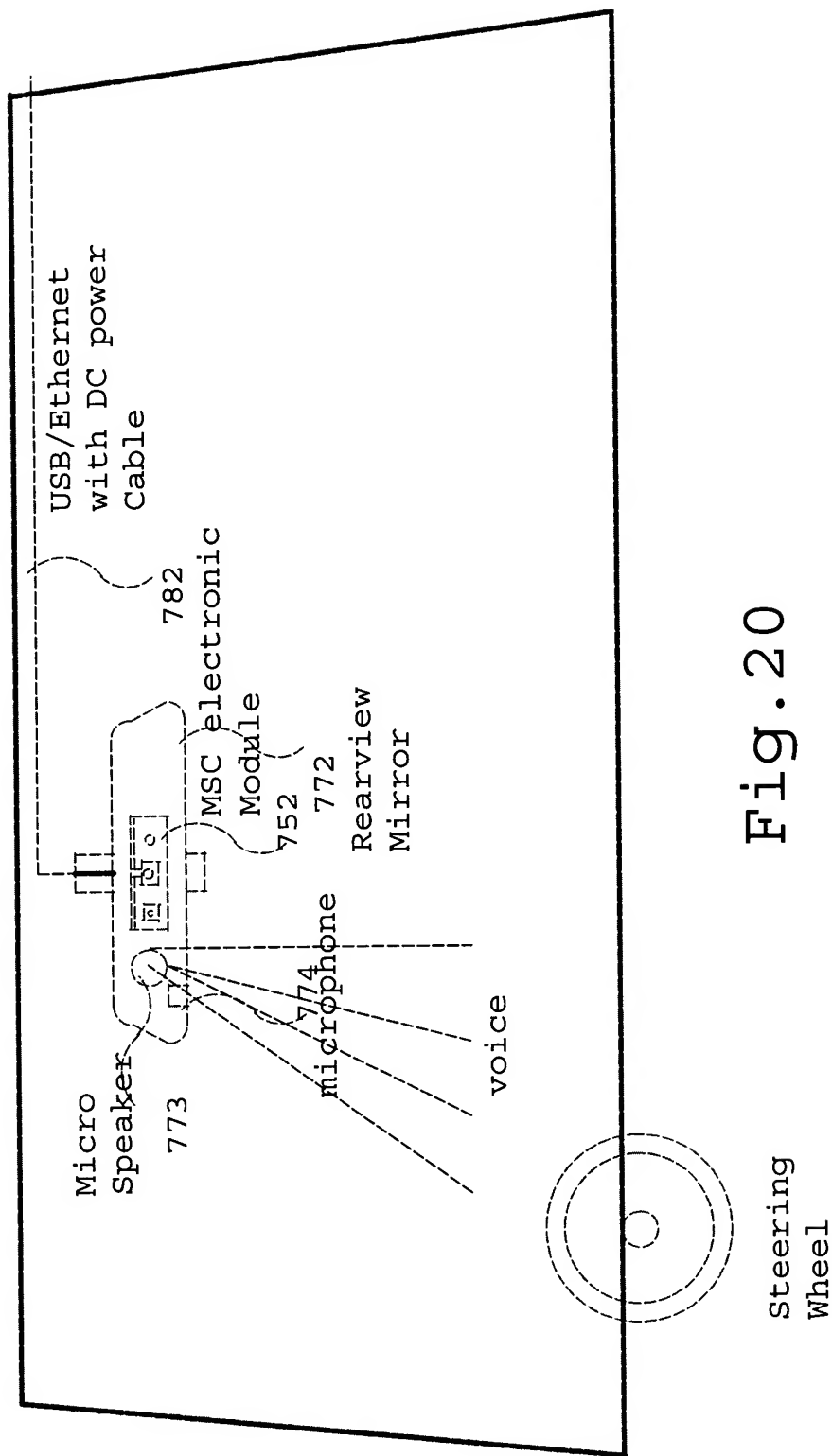


Fig. 20

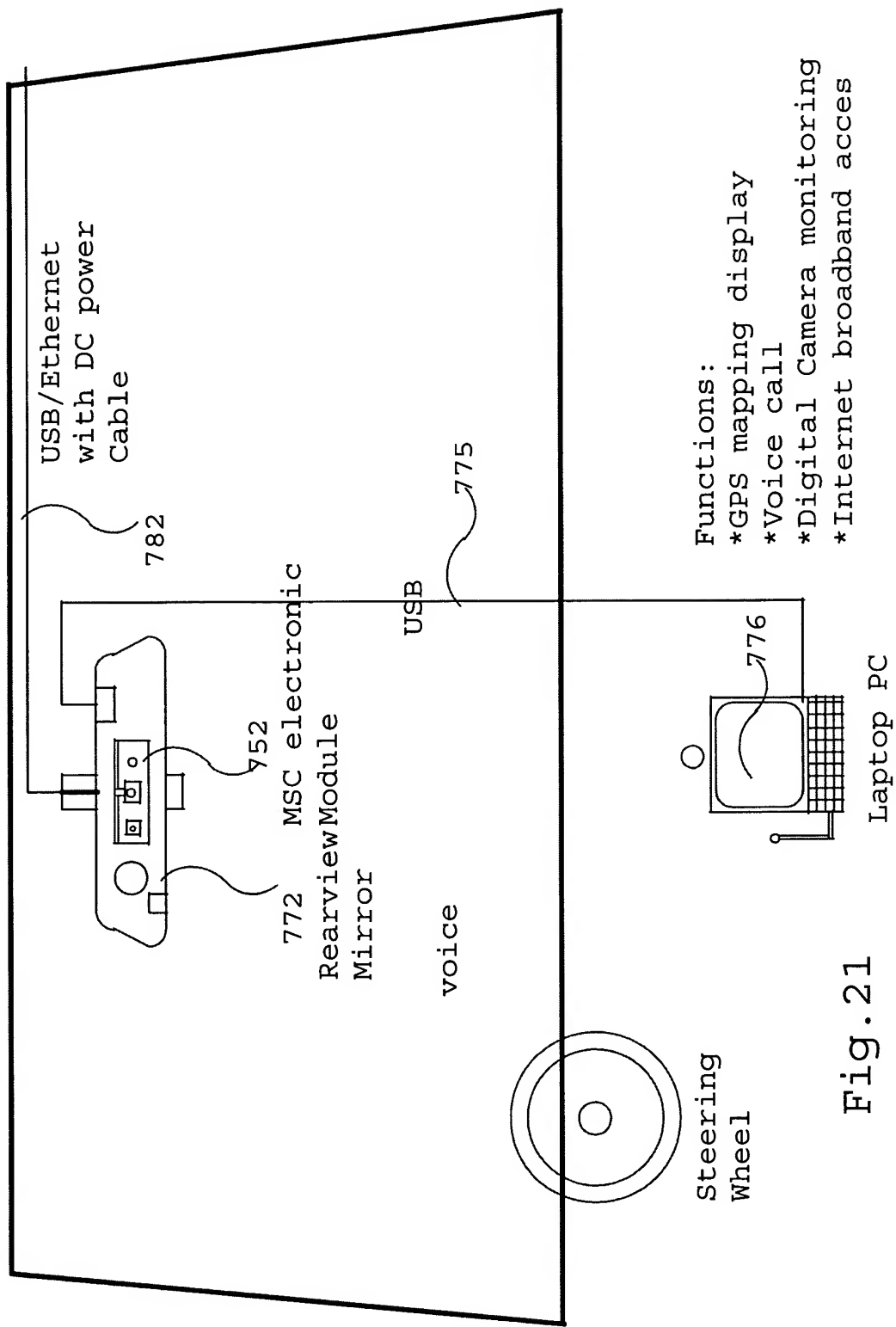


Fig. 21

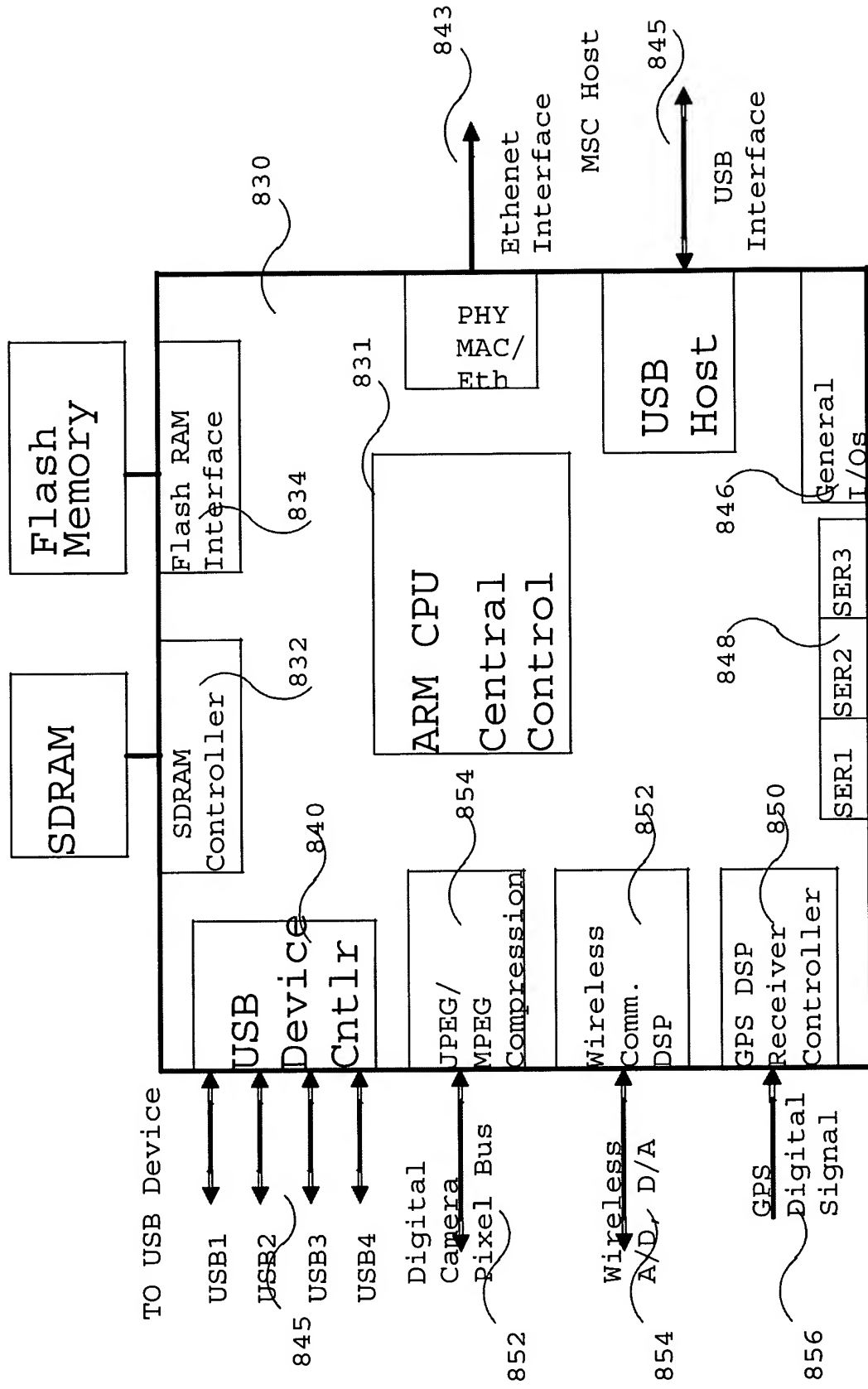


Fig. 22

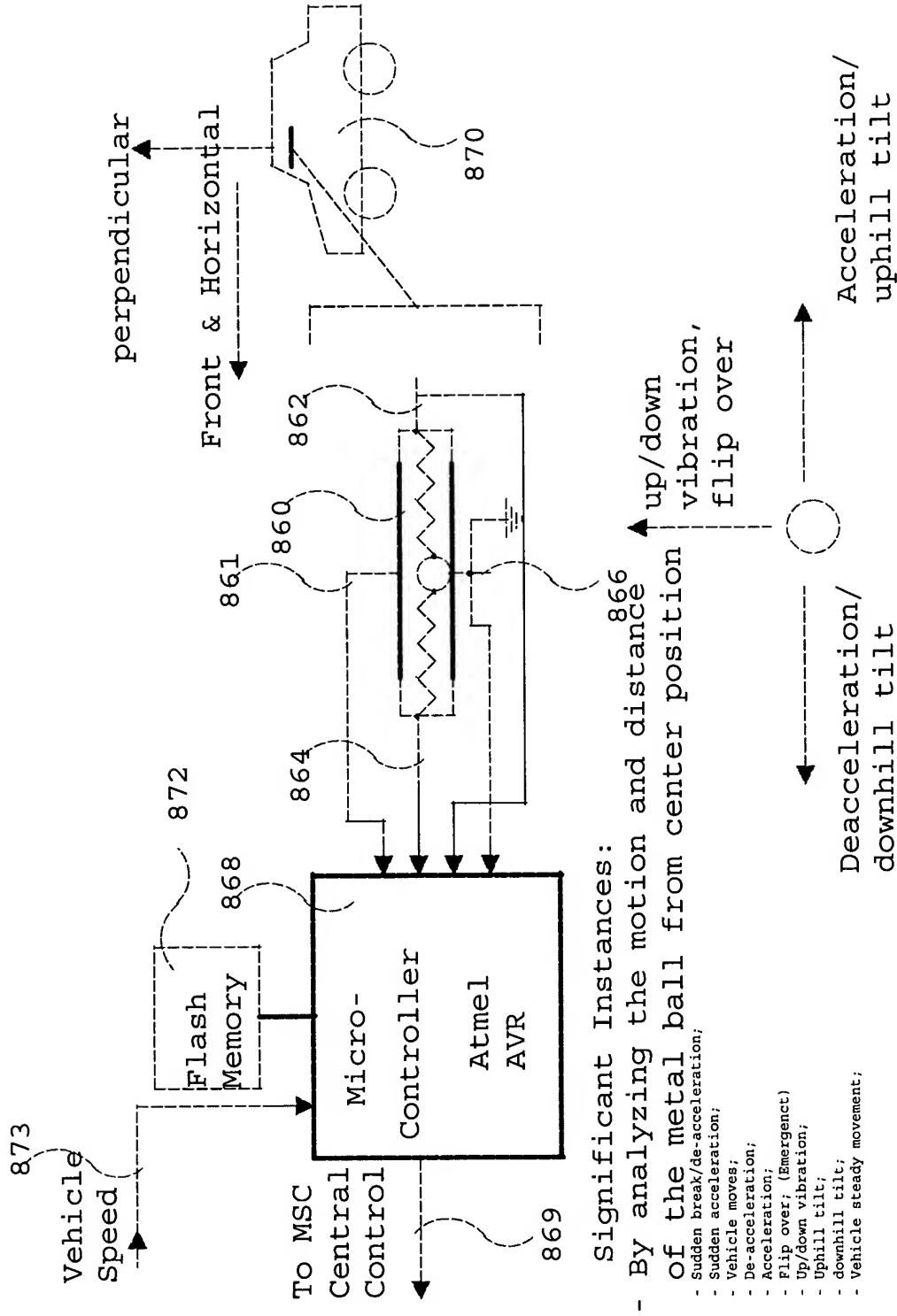


Fig.23